What is claimed is:

1. A controller for an optical disk drive comprising:

a modulator configured to modulate record data to be recorded on an optical disk based on a record clock which is a reference clock for recording, and to generate modulation data and address information of the modulation data;

a prepit decoder configured to generate a prepit clock from a prepit signal detected from the optical disk; and

a decision circuit configured to determine whether recording in accordance with a standard is performed, from a phase characteristic based on the address information and the prepit clock, and to control a frequency of the record clock.

2. The controller of claim 1, wherein the prepit decoder comprises a prepit slicer configured to generate the prepit clock by subjecting the prepit signal to waveform shaping.

3. The controller of claim 1, further comprising:

a wobble PLL configured to generate a wobble clock based on a wobble signal detected from the optical disk; and

a record clock generator configured to generate the record clock.

4. The controller of claim 3, wherein the modulator comprises:

a wobble counter configured to generate a sector synchronization signal by counting the wobble clock;

a timing controller configured to generate a timing signal in synchronization with either one of the sector synchronization signal and a reproducing synchronization signal

obtained from previously recorded data on the optical disk;

an encode address counter configured to generate a modulation control signal and the address information by counting the record clock when the timing signal is effective; and

a modulation data generator configured to modulate the record data based on the modulation control signal.

5. The controller of claim 4, wherein the wobble counter further generates a sector pulse by an interval of a sector of the optical disk.

6. The controller of claim 4, wherein the decision circuit comprises:

an address register configured to latch the address information in synchronization with the prepit clock;

a dividing correction circuit configured to generates a dividing correction signal based on latched address information; and

a dividing correction register configured to latch the dividing correction signal when the timing signal is effective.

7. The controller of claim 6, wherein the dividing correction circuit comprises:

a decoder configured to generate the phase characteristic from the latched address information; and

a window circuit configured to generate the dividing correction signal by comparing the phase characteristic to a window value.

8. The controller of claim 7, wherein the window circuit has a positive window value

and a negative window value as the window value

9. The controller of claim 6, wherein the record clock generator comprises:

a dividing setting register configured to generate a reference dividing signal in accordance with a command;

an adder configured to generate a dividing control signal by adding the reference dividing signal and the dividing correction signal; and

a PLL configured to generate the record clock based on the dividing control signal.

10. The controller of claim 9, wherein the PLL comprises:

a VCO configured to generate an oscillation clock by oscillating at a frequency corresponding to a control voltage;

a programmable counter configured to change a dividing ratio by applying the dividing control signal, and to divide the oscillation clock;

a first divider configured to generate a dividing clock by dividing either of a reference clock and the wobble clock;

a phase comparator configured to generate the control voltage in accordance with a phase difference between the divided oscillation clock and the dividing clock;

a loop filter configured to extract a low frequency component of the control voltage, and to supply the low frequency component to the VCO; and

a second divider configured to generate the record clock by dividing the oscillation clock.

11. The controller of claim 5, wherein the decision circuit comprises:

an address register configured to latch the address information in synchronization

with the sector pulse;

a dividing correction circuit configured to generates a dividing correction signal based on latched address information; and

a dividing correction register configured to latch the dividing correction signal when the timing signal is effective.

12. The controller of claim 11, wherein the dividing correction circuit comprises:

a decoder configured to generate the phase characteristic from the latched address information; and

a window circuit configured to generate the dividing correction signal by comparing the phase characteristic to a window value.

13. The controller of claim 12, wherein the window circuit has a positive window value and a negative window value as the window value.

14. The controller of claim 11, wherein the record clock generator comprises:

a dividing setting register configured to generate a reference dividing signal in accordance with a command;

an adder configured to generate a dividing control signal by adding the reference dividing signal and the dividing correction signal; and

a PLL configured to generate the record clock based on the dividing control signal.

15. The controller of claim 14, wherein the PLL comprises:

a VCO configured to generate an oscillation clock by oscillating at a frequency corresponding to a control voltage;

a programmable counter configured to change a dividing ratio by use of the dividing control signal, and to divide the oscillation clock;

a first divider configured to generate a dividing clock by dividing either a reference clock and the wobble clock;

a phase comparator configured to generate the control voltage in accordance with a phase difference between the divided oscillation clock and the dividing clock;

a loop filter configured to extract a low frequency component of the control voltage, and to supply the low frequency component to the VCO; and

a second divider configured to generate the record clock by dividing the oscillation clock.

16. The controller of claim 5, wherein the decision circuit comprises:

a first address register configured to latch the address information in synchronization with the prepit clock, and to generate a first latch signal;

a second address register configured to latch the address information in synchronization with the sector pulse and to generate a second latch signal;

a dividing correction circuit configured to generate a dividing correction signal based on the first and second latch signals; and

a dividing correction register configured to latch the dividing correction signal when the timing signal is effective.

17. The controller of claim 16, wherein the dividing correction circuit comprises:

a first decoder configured to generate a first phase characteristic as the phase characteristic from the first latch signal;

a second decoder configured to generate a second phase characteristic as the phase

characteristic from the second latch signal;

a first window circuit configured to compare the first phase characteristic to a window value, and to generate a first dividing correction signal;

a second window circuit configured to compare the second phase characteristic to a window value, and to generate a second dividing correction signal; and

a window decision circuit configured to select either one of the first and second dividing correction signals.

18. The controller of claim 17, wherein the record clock generator comprises:

a dividing setting register configured to generate a reference dividing signal in accordance with a command;

an adder configured to generate a dividing control signal by adding up the reference dividing signal and the dividing correction signal; and

a PLL configured to generate the record clock based on the dividing control signal.

19. A semiconductor integrated circuit comprising:

a modulator integrated on a semiconductor chip and configured to modulate a record data to be recorded on a optical disk based on a record clock that is a reference clock for recording, and to generate a modulation data and an address information of the modulation data;

a prepit decoder integrated on the semiconductor chip and configured to generate a prepit clock from a prepit signal detected from the optical disk; and

a decision circuit integrated on the semiconductor chip and configured to determine whether or not recording in accordance with a standard is performed, from phase characteristic based on the address information and the prepit clock, and to control a

frequency of the record clock.

20. An optical disk drive comprising:

a pickup configured to read light reflected from an optical disk, the reflected light generated by irradiating a laser beam on the optical disk, and to generate a prepit signal and a wobble signal;

a controller configured to determine whether recording in accordance with an established standards is performed, from phase characteristic based on the prepit signal and the wobble signal, and to modulate record data to be recorded on the optical disk; and

a signal processor configured to supply the record data to the controller.